IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A method for fabricating a non-volatile memory, comprising:

providing a substrate with a stacked structure having a control gate, a barrier layer, a trapping layer, and a tunneling layer, wherein an anti-reflection layer covers the stacked structure on top;

forming an oxide layer on an exposed surface of the of the control gate;

forming an insulating spacer on a sidewall of the stacked structure, and covering the oxide layer; and

performing a plasma enhanced chemical vapor deposition process to form ~~forming~~ an ultraviolet-resistant lining layer over the surface of the stacked structure, wherein the ultraviolet-resistant lining layer can effectively resist ultraviolet light.

2. (original) The method of claim 1, wherein the insulating spacer is a silicon oxide spacer.

3. (original) The method of claim 1, wherein the ultraviolet-resistant lining layer is a silicon nitride lining layer.

4. (currently amended) The method of claim 3, wherein the step of forming the silicon nitride lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 370W and 410W, ~~the PECVD~~ using a reacting gas including a SiH_4 gas with a flow rate between 50 sccm and 60 sccm, ~~an~~ ammonia (NH_3) gas and a nitrogen (N_2) gas.

5. (currently amended) The method of claim 1, wherein the anti-reflection layer includes inorganic material, ~~so that~~ and the anti-reflection layer ~~is not removed during removing the photoresist layer and the oxide layer is formed on sidewalls of~~ serves to protect the control gate.

6. (currently amended) The method of claim 1, wherein the anti-reflection layer includes organic material, ~~so that~~ and the anti-reflection layer is ~~simultaneously~~ subsequently removed ~~during removing the photoresist layer and the oxide layer is formed on top and sidewalls of the control gate.~~

7. (original) The method of claim 1, wherein the oxide layer is formed by performing a thermal oxidation process.

8. (original) The method of claim 1, further forming a source/drain region in the substrate at each side of the stacked structure.

9. (currently amended) A fabrication process for metal interconnects, comprising:

providing a substrate, the substrate having a conducting structure;

forming a dielectric layer on the substrate to cover the conducting structure;

forming a contact window in the dielectric layer, the contact window being electrically connected to the conducting structure;

forming a conducting line structure on the dielectric layer, the conducting line structure being electrically connected to the contact window; and

performing a plasma enhanced chemical vapor deposition process to form ~~forming~~ a low surface charge lining layer ~~on surfaces of the dielectric layer and~~ for

covering the conducting line structure, wherein the low surface charge lining layer can effectively resist ultraviolet light.

10. (original) The method of claim 9, wherein the low surface charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer.

11. (currently amended) The method of claim 10, wherein the step of forming the silicon oxide lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 80W and 120W, ~~the PECVD using~~ a reacting gas including a silane (SiH_4) gas with a flow rate between 20sccm and 30sccm, and a nitrous (N_2O) gas.

12. (original) The method of claim 9, further comprising forming a second dielectric layer on the low surface charge lining layer.

13. (currently amended) A method for fabricating a non-volatile memory, comprising:

sequentially forming a tunneling layer, a trapping layer, a barrier layer, a gate conductive layer, and an anti-reflection layer on a substrate;

forming a patterned photoresist layer ~~with a pattern~~ on the anti-reflection layer;

using the patterned photoresist layer as a mask to etch the anti-reflection layer, the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer, to form a stacked structure having a control gate, the barrier layer, the trapping layer, and the tunneling layer, wherein the anti-reflection layer covers the stacked structure ~~on top~~;

removing the patterned photoresist layer;

forming an oxide layer on an exposed surface of the ~~of the~~ control gate;

forming a source/drain region in the substrate at each side of the stacked structure;

performing a plasma enhanced chemical vapor deposition process to form ~~forming~~ an ultraviolet-resistant lining layer over the stacked structure, wherein the ultraviolet-resistant lining layer can effectively resist ultraviolet light;

forming a dielectric layer on the ultraviolet-resistant lining layer;

forming a contact window in the dielectric layer, the contact window being electrically connected to the control gate;

forming a conducting line structure on the dielectric layer, the conducting line structure being electrically connected to the contact window; and

forming a low-surface-charge lining layer over the dielectric layer and the conducting line structure.

14. (currently amended) The method of claim 13, further comprising a step of forming an insulating spacer covering the oxide layer, wherein the insulating spacer is a silicon oxide spacer.

15. (original) The method of claim 13, wherein the ultraviolet-resistant lining layer is a silicon nitride lining layer.

16. (currently amended) The method of claim 15, wherein the step of forming the silicon nitride lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 370W and 410W, ~~the PECVD~~ using a reacting gas including a silane (SiH_4) gas with a flow rate

between 50sccm and 60sccm, ~~an ammonium~~ ammonia (NH_3) gas and ~~a nitroge~~ nitrogen (N_2) gas.

17. (original) The method of claim 13, wherein the low-surface-charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer.

18. (original) The method of claim 17, wherein the step of forming the silicon oxide lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 80W and 120W, ~~the PECVD~~ using a reacting gas including a SiH_4 gas with a flow rate between 20sccm and 30sccm, and an NO_2 gas.

19. (currently amended) The method of claim 13, wherein the anti-reflection layer includes inorganic material, ~~so that~~ and the anti-reflection layer is ~~not removed during removing the photoresist layer and the oxide layer is formed on sidewalls of~~ retained to protect the control gate.

20. (currently amended) The method of claim 13, wherein the anti-reflection layer includes organic material, ~~so that~~ and the anti-reflection layer is removed simultaneously ~~removed~~ during the step of removing the patterned photoresist layer and the oxide layer ~~is formed on top and sidewalls of the control gate.~~

21. (original) The method of claim 13, wherein the oxide layer is formed by performing a thermal oxidation process.

22. (original) The method of claim 13, further comprising forming a second dielectric layer on the low-surface-charge lining layer.